

ACKNOWLEDGEMENT RECEIPT

Electronic Version

Stylesheet Version v01

Title of Invention

A SYSTEM AND METHOD OF PROVIDING ERROR DETECTION
AND CORRECTION CAPABILITY IN AN INTEGRATED CIRCUIT
USING REDUNDANT LOGIC CELLS OF AN EMBEDDED FPGA

Submission Type : Utility Patent Filing

Application Number:

10/709754



EFS ID:

61574

Server Response:

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ISVR1	Submission was successfully submitted - Even if Informational or Warning Messages appear below, please do not resubmit this application
ICON1	3753
WGEN24	Filename= all XMLs having <invention-title> BusinessRule= Common elements across multiple XML documents within the submission package do not have synchronized data content. #Supporting Msg:<invention-title> not the same or having font format.

First Named Applicant: JOHN COHN

Attorney Docket Number: BUR920040001US1

Timestamp: 2004-05-26 16:22:11 EDT

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File Listing:

Doc. Name	File Name	Size (Bytes)	Date Produced (yyyymmdd)
us-fee-sheet	BUR920040001US1-usfees.xml	2087	2004-05-26
us-fee-sheet	us-fee-sheet.xml	24912	2004-05-26
us-fee-sheet	us-fee-sheet.dtd	11069	2004-05-26
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application-body	wipo.ent	4956	2004-05-26
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application-body	isoamsa.ent	5191	2004-05-26
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